IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently Amended): A power semiconductor device comprising:

a semiconductor active layer;

a first base layer of a first conductivity type disposed in the active layer;

a plurality of trenches disposed in a surface of the active layer at intervals to partition a main cell and a dummy cell, and to reach the first base layer;

a collector layer of a second conductivity type disposed on the first base layer, at a position remote from the trenches;

a second base layer of the second conductivity type disposed in the main cell and on the first base layer;

an emitter layer of the first conductivity type disposed on the second base layer;

a buffer layer of the second conductivity type disposed in the dummy cell and on the first base layer;

a gate electrode disposed in each trench to face, through a gate insulating film, a portion of the second base layer sandwiched between the first base layer and the emitter layer;

a collector electrode disposed on the collector layer;

an emitter electrode disposed on the second base layer and the emitter layer; and

a partition structure disposed in the surface of the active layer to electrically isolate the buffer layer from the emitter electrode,

wherein the partition structure comprises dummy cell end walls, which bridge ends of the trenches one on either end of the dummy cell and cooperate with the trenches to surround the dummy cell.

Claim 2 (Currently Amended): The device according to claim 1, wherein the dummy cell end walls comprise ~~partition structure comprises a partition wall formed of~~ a partition trench disposed in the surface of the active layer.

Claim 3 (Original): The device according to claim 2, wherein the partition trench has a depth substantially the same as the trenches.

Claim 4 (Original): The device according to claim 2, further comprising a conductive layer disposed in the partition trench and wrapped in an insulating film, wherein the conductive layer is electrically connected to the gate electrode.

Claim 5 (Original): The device according to claim 2, wherein the partition trench is filled with an insulating layer.

Claim 6 (Currently Amended): The device according to claim 1, wherein the dummy cell end walls comprise ~~partition structure comprises a partition wall formed of~~ a partition layer of the first conductivity type disposed in the surface of the active layer.

Claim 7 (Canceled).

Claim 8 (Currently Amended): The device according to claim 1, wherein the dummy cell end walls comprise ~~partition structure comprises a partition wall formed of~~ a combination of a partition trench and a partition layer of the first conductivity type, the partition trench being disposed in the surface of the active layer, and the partition layer of the first

conductivity type being disposed in the active layer at a position deeper than the partition trench.

Claims 9-20 (Canceled).

Claim 21 (New): A power semiconductor device comprising:

a semiconductor active layer;

a first base layer of a first conductivity type disposed in the active layer;

a plurality of trenches disposed in a surface of the active layer at intervals to partition a main cell and a dummy cell, and to reach the first base layer;

a collector layer of a second conductivity type disposed on the first base layer, at a position remote from the trenches;

a second base layer of the second conductivity type disposed in the main cell and on the first base layer;

an emitter layer of the first conductivity type disposed on the second base layer;

a buffer layer of the second conductivity type disposed in the dummy cell and on the first base layer;

a gate electrode disposed in each trench to face, through a gate insulating film, a portion of the second base layer sandwiched between the first base layer and the emitter layer;

a collector electrode disposed on the collector layer;

an emitter electrode disposed on the second base layer and the emitter layer; and

a partition structure disposed in the surface of the active layer to electrically isolate the buffer layer from the emitter electrode,

wherein the partition structure comprises main cell end walls, which bridge ends of the trenches one on either end of the main cell and cooperate with the trenches to surround the main cell.

Claim 22 (New): The device according to claim 21, wherein the main cell end walls comprise a partition trench disposed in the surface of the active layer.

Claim 23 (New): The device according to claim 22, wherein the partition trench has a depth substantially the same as the trenches.

Claim 24 (New): The device according to claim 22, further comprising a conductive layer disposed in the partition trench and wrapped in an insulating film, wherein the conductive layer is electrically connected to the gate electrode.

Claim 25 (New): The device according to claim 22, wherein the partition trench is filled with an insulating layer.

Claim 26 (New): The device according to claim 21, wherein the main cell end walls comprise a partition layer of the first conductivity type disposed in the surface of the active layer.

Claim 27 (New): The device according to claim 21, wherein the main cell end walls comprise a combination of a partition trench and a partition layer of the first conductivity type, the partition trench being disposed in the surface of the active layer, and the partition

layer of the first conductivity type being disposed in the active layer at a position deeper than the partition trench.

Claim 28 (New): A power semiconductor device comprising:

a semiconductor active layer;

a first base layer of a first conductivity type disposed in the active layer;

a plurality of trenches disposed in a surface of the active layer at intervals to partition a main cell and a dummy cell, and to reach the first base layer;

a collector layer of a second conductivity type disposed on the first base layer, at a position remote from the trenches;

a second base layer of the second conductivity type disposed in the main cell and on the first base layer;

an emitter layer of the first conductivity type disposed on the second base layer;

a buffer layer of the second conductivity type disposed in the dummy cell and on the first base layer;

a gate electrode disposed in each trench to face, through a gate insulating film, a portion of the second base layer sandwiched between the first base layer and the emitter layer;

a collector electrode disposed on the collector layer;

an emitter electrode disposed on the second base layer and the emitter layer; and

a partition structure disposed in the surface of the active layer to electrically isolate the buffer layer from the emitter electrode,

wherein the partition structure comprises a partition wall including a partition layer of the first conductivity type disposed in the surface of the active layer.

Claim 29 (New): The device according to claim 28, wherein the partition layer comprises a portion integral with the first base layer.

Claim 30 (New): The device according to claim 28, wherein the partition wall is formed of a combination of a partition trench and the partition layer of the first conductivity type, the partition trench being disposed in the surface of the active layer, and the partition layer of the first conductivity type being disposed in the active layer at a position deeper than the partition trench.

Claim 31 (New): The device according to claim 30, wherein the partition trench has a depth substantially the same as the trenches.

Claim 32 (New): The device according to claim 30, further comprising a conductive layer disposed in the partition trench and wrapped in an insulating film, wherein the conductive layer is electrically connected to the gate electrode.

Claim 33 (New): The device according to claim 30, wherein the partition trench is filled with an insulating layer.